CLAIMS

What is claimed is:

1. A content addressable memory (CAM) device comprising:

a CAM array including a plurality of CAM cells arranged in rows and columns, a plurality of bit lines coupled respectively to the columns of CAM cells, and a plurality of comparand lines coupled respectively to the columns of CAM cells, the plurality of comparand lines being adapted to provide, as part of a compare operation, a comparand value for comparison with data words stored in the rows of CAM cells;

an error detection circuit coupled to receive, via the bit lines, a selected data word from one of the rows of CAM cells and to determine, concurrently with the compare operation, whether the selected data word includes an error.

2. The CAM device of claim 1 wherein the error detection circuit includes circuitry to assert an error signal if the selected data word includes an error.

3. The CAM device of claim 2 wherein the CAM array further includes storage cells to store a plurality of validity values, each validity value indicating whether a respective row of CAM cells contains a valid data word, the circuitry to assert the error signal being coupled to receive one of the validity values that corresponds to the selected data word and including circuitry to prevent assertion of the error signal if the one of the validity values indicates that the selected data word is not a valid data word.

4. The CAM device of claim 1 further comprising:

an address generator to generate an error check address; and

an address decoder coupled to receive the error check address from the address generator, the address decoder including circuitry to assert, according to the error check address, one of a plurality of signals to enable the one of the rows of CAM cells to output the selected data word onto the bit lines.

5. The CAM device of claim 4 wherein the error detection circuit is coupled to the address generator to receive the error check address therefrom, the error detection circuit including a storage circuit to store the error check address in response to a determination that the selected data word includes an error.

6. The CAM device of claim 4 further comprising:

an address selector coupled between the address generator and the address decoder;

a control circuit coupled to the address selector and having an input to receive instructions from a host, the control circuit being adapted to determine, for a given time interval, whether execution of one or more of the instructions requires use of the bit lines within the CAM array and to signal the address selector to select the address generator as an address source if use of the bit lines is not required for execution of the one or more of the instructions.

7. The CAM device of claim 1 further comprising a read circuit coupled to the bit lines and to the error detection circuit, the read circuit including sense amplifiers to sense respective bits of the selected data word and to output the selected data word to the error detection circuit.

8. The CAM device of claim 1 wherein the error detection circuit includes circuitry to

determine whether the selected data word has a parity error.

9. The CAM device of claim 1 wherein the error detection circuit includes circuitry to determine, if the selected data word includes an error, which bit of the selected data word is in error.

10. The CAM device of claim 1 wherein the CAM array further includes storage cells to store a plurality of validity values, each validity value indicating whether a respective row of the CAM cells contains a valid data word, and wherein the CAM device further comprises a write circuit to set one of the validity values to a first state to indicate that the one of the rows of CAM cells does not contain a valid word if the error detection circuit determines that the selected data word includes an error.

11. The CAM device of claim 1 wherein each of the plurality of CAM cells is a ternary CAM cell.

12. The CAM device of claim 11 wherein the selected data word is a local mask value.

13. The CAM device of claim 11 wherein the selected data word is a CAM word.

14. The CAM device of claim 1 further comprising:

an error correction circuit to correct an error in the selected data word to generate a corrected data word; and

a write circuit to write the corrected data word into the one of the rows of CAM cells.

15. The CAM device of claim 1 further comprising:

circuitry to generate an error check value based on an input data word; and

circuitry to store the error check value and the input data word in the CAM array.

16. A content addressable memory (CAM) device comprising:

a CAM array including:

CAM cells arranged in rows and columns, each row of the CAM cells being adapted to store a respective data word;

validity storage cells to store validity values, each validity value corresponding to a respective row of the CAM cells and indicating whether a valid data word is stored therein; and

bit lines coupled to respective columns of the CAM cells, including at least one bit line coupled to the validity storage cells; and

an error detection circuit coupled to receive, via the bit lines, a selected data word from a selected one of the rows of CAM cells and a corresponding validity value, the error detection circuit including a first circuit to determine whether the selected data word includes an error, and a second circuit, responsive to an error indication from the first circuit, to output an error signal if the selected data word is determined to include an error, the second circuit including an input to receive the validity value that corresponds to the selected data word and being adapted to prevent assertion of the error signal if the validity value indicates that the selected data word is not a valid data word.

17. The CAM device of claim 16 wherein the error detection circuit includes a parity checking circuit to detect whether the selected data word includes a parity error.

18. The CAM device of claim 16 wherein the first circuit is adapted to determine which bit of the selected data word is in error, if any.

19. The CAM device of claim 16 wherein each of the CAM cells is a ternary CAM cell and wherein the selected data word is a local mask word.

20. The CAM device of claim 16 wherein each of the CAM cells is a ternary CAM cell and wherein the selected data word is a CAM word.

21. A content addressable memory (CAM) device comprising:

a CAM array including a plurality of rows of CAM cells and a plurality of validity storage cells; and

an error detection circuit coupled to the CAM array to receive a data word from a selected one of the rows of CAM cells and to receive a corresponding validity value from one of the validity storage cells.

22. The CAM device of claim 21 wherein the second circuit is an AND logic gate having a first input coupled to receive the validity value and a second input coupled to receive an error indication from the first circuit.

23. The CAM device of claim 21 wherein the error detection circuit comprises:

a first circuit to determine if the data word includes an error; and

a second circuit coupled to the first circuit and coupled to receive the validity value, the second circuit being configured to output an error signal if the first circuit determines that the data word includes an error and if the validity value indicates that the data

word is a valid data word.

24. The CAM device of claim 21 wherein the first circuit includes a parity generation circuit to generate a parity value based on the CAM word.

25. The CAM device of claim 24 wherein the first circuit further includes a compare circuit to compare the parity value generated by the parity generation circuit with a parity value that corresponds to the selected one of the rows of CAM cells.

26. The CAM device of claim 21 wherein the CAM cells are ternary CAM cells.

27. A content addressable memory (CAM) device comprising:

a CAM array including a plurality of CAM cells arranged in rows and columns, and a plurality of bit lines coupled respectively to the columns of CAM cells;

an address generator to output a plurality of error check addresses in a predetermined sequence;

an address decoder coupled to the CAM array and coupled to the address generator to receive the plurality of error check addresses therefrom, the address decoder including circuitry to select, according to each error check address, one of the rows of CAM cells; and

an error detection circuit coupled to receive, via the bit lines, a data word from the selected one of the rows of CAM cells and to determine whether the data word includes an error.

28. The CAM device of claim 27 further comprising an error address register coupled to receive the error check address from the address generator and coupled to receive an error

indication from the error detection circuit, the error address register being adapted to store the error check address if the error indication from the error detection circuit indicates that the data word includes an error.

29. The CAM device of claim 28 wherein the error address register is a multiple-entry register to store error check addresses one after another in response to successive error indications from the error detection circuit.

30. The CAM device of claim 28 wherein the error address register outputs an error address signal to be read by a host device.

31. The CAM device of claim 28 further comprising an error correction circuit to generate a corrected data word by correcting an error detected in the data word, and wherein the error address register is loaded with the error check address and the corrected data value in response to the error indication.

32. The CAM device of claim 28 wherein the plurality of error check addresses are output in a predetermined sequence to systematically check the plurality of CAM cells for errors.

33. The CAM device of claim 27 further comprising a configuration register to store a configuration value, and wherein the predetermined sequence is determined according to the configuration value.

34. The CAM device of claim 27 further comprising a configuration register to store a configuration value, and wherein the error detection circuit is a parity check circuit having an input coupled to receive the configuration value from the configuration register, the

parity check circuit being adapted to test the data word for either even parity or odd parity according to the configuration value

35. A method of operation within a content addressable memory (CAM) device, the method comprising:

comparing a comparand with a plurality of data words stored within the CAM device in a compare operation; and

determining, concurrently with the compare operation, whether a selected one of the data words includes an error.

36. The method of claim 35 wherein determining whether a selected one of the plurality of data words includes an error comprises determining whether a selected one of the data words has a parity error.

37. The method of claim 35 further comprising generating an address in an address generator within the CAM device to select the selected one of the data words.

38. The method of claim 37 further comprising incrementing the address generator to select another of the data words in response to determining that the selected one of the data words does not include an error.

39. The method of claim 37 further comprising storing the address in an error address register in response to determining that the selected one of the data words includes an error.

40. The method of claim 35 further comprising outputting an error signal from the CAM device in response to determining that the selected one of the data words includes an error.

41. A method of operation within a content addressable memory (CAM) device, the method comprising:

determining whether a selected data word within a CAM array of the CAM device includes an error; and

asserting an error signal if the selected data word is determined to include an error and if a validity value that corresponds to the selected data word indicates that the selected data word is a valid data word.

42. The method of claim 41 further comprising preventing assertion of the error signal, regardless of whether the selected data word is determined to include an error, if the validity value indicates that the selected data word is not a valid data word.

43. The method of claim 41 wherein preventing assertion of the error signal regardless of whether the selected data word is determined to include an error comprises generating a first signal indicative of whether the selected data word includes an error and gating the first signal in a logical AND gate according to whether the validity value indicates that the selected data word is a valid data word.

44. The method of claim 41 wherein determining whether a selected data word includes an error comprises:

generating a parity bit based on the selected data word ; and

comparing the parity bit with a parity bit stored in the CAM array.

45. The method of claim 41 wherein determining whether a selected data word includes an error comprises:

generating a syndrome value based on an error code stored in the CAM array and the selected data word; and

determining whether any bit of the syndrome value has a different state than any other bit of the syndrome value.

46. A method of controlling a content addressable memory (CAM) device, the method comprising:

receiving from the CAM device, an address of a storage location within the CAM device that contains a corrupted data value; and

outputting a write instruction and write data to the CAM device to overwrite the corrupted data value.

47. The method of claim 46 further comprising:

receiving an error signal from the CAM device indicating detection of the corrupted data value; and

outputting a first instruction to the CAM device, the first instruction instructing the CAM device to output the address of the storage location that contains the corrupted data value.

48. The method of claim 46 further comprising retrieving the write data from a backup storage according to the address of the storage location within the CAM device that contains the corrupted data value.

49. A system comprising:

a plurality of signal lines;

a processor coupled to the plurality of signal lines; and

a CAM device coupled to the plurality of signal lines, the CAM device including an error checking circuit to automatically determine whether any of a plurality of data values stored within the CAM device has an error and to signal the processor via one or more of the plurality of signal lines in response to detecting the error.

50. The system of claim 49 wherein the processor is a network processor.

51. The system of claim 49 wherein the error checking circuit includes a parity checking circuit to determine whether any of the plurality of data values stored within the CAM device has a parity error.

52. The system of claim 51 wherein the error checking circuit is configured to store, in response determining that one of the plurality of data values has an error, an error address indicative of a storage location within the CAM device in which the one of the plurality of data values is stored.

53. The system of claim 52 wherein the error checking circuit is further configured to output the error address to the processor in response to determining that one of the plurality of data values has an error.

54. The system of claim 52 wherein the processor is configured to issue an instruction to the CAM device upon receiving the signal from the CAM device, the instruction instructing the CAM device to output the error address to the processor.

55. The system of claim 52 further comprising a backup storage coupled to the processor, the

processor being configured to obtain the error address from the CAM device and to access the backup storage according to the error address to obtain a write data value, the processor further being configured to output the write data value and a write instruction to the CAM device.

56. The system of claim 55 wherein the CAM device is configured to receive the write data value and the write instruction from the CAM device and, in response to receiving the write data value and the write instruction, to store the write data value at the error address.

57. A content addressable memory (CAM) device comprising:
an array of CAM cells for storing data words; and
detecting means for detecting when a valid one of the data words has an error.

58. The CAM device of claim 57 further comprising means for comparing comparand data with the data words concurrently with the detecting means detecting when the valid one of the data words has an error.

59. The CAM device of claim 57 wherein the detecting means for detecting when a valid one of the data words has an error comprises means for determining whether a validity indicator associated with the one of the data words indicates that the one of the data words is valid.

60. The CAM device of claim 57 wherein the detecting means for detecting when a valid one of the data words has an error comprises means for detecting a parity error.

61. The CAM device of claim 57 further comprising:

means for generating a first error check value;

means for storing the first error check value in the CAM device; and

wherein the detecting means includes means for generating a second error check value and means for comparing the first error check and the second error check value to detect when the valid one of the data words has an error.

62. The CAM device of claim 57 further comprising address generating means for generating a sequence of check addresses, including an address that corresponds to the valid one of the data words.

63. The CAM device of claim 57 further comprising:

means for generating an error check value based on an input data word; and

means for storing the error check value and the input data word in the array of CAM cells.

64. A content addressable memory (CAM) device comprising:

an array of CAM cells for storing data words; and

means for concurrently (i) determining when the array stores a data word that has an error, and (ii) comparing comparand data with the data words.

65. The CAM device of claim 64 further comprising address generating means for generating a sequence of check addresses for systematically checking the data words for error.

66. The CAM device of claim 64 wherein the means for determining when the array stores a data word that has an error comprises means for detecting a parity error in the data word.

67. The CAM device of claim 64 further comprising means to configure a width and depth of

the CAM array.